In the Claims

Claims 1-7 and 21-30 have been canceled without prejudice. Claims 8-20 and 31-50 remain in the application.

8. (Amended) A method of forming a pair of field effect transistors comprising:

forming a pair of active areas over a substrate, one of the active areas having a width less than one micron;

forming a gate line over both active areas to provide a pair of transistors having different threshold voltages, the transistors being provided with the different threshold voltages without using a separate channel implant for either transistor; and

wherein the transistor with [the] a lower of the threshold voltages corresponds to the active area having the width less than one micron.

9. (Amended) The method of claim 8 further comprising forming the transistor having [the] a higher of the threshold voltages to have an active area width greater than one micron.

10. (Amended) The method of claim 8 further comprising forming the transistor having [the] a higher of the threshold voltages to have an active area width less than one micron.

13. (Amended) The method of claim 8, wherein the forming of the gate line comprises forming a common gate line over the pair of active areas.

14. (Amended) The method of claim 8, wherein the forming of the gate line comprises forming a common gate line over the pair of active areas, the transistors being formed in a parallel configuration.

31. (Amended) A semiconductor processing method of forming dynamic random access memory circuitry comprising:

providing a substrate having a memory array area over which memory circuitry is to be formed, and a peripheral area over which peripheral circuitry is to be formed;

forming a plurality of shallow trench isolation regions received within the peripheral area of the substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths within the substrate, some of the widths being no greater than about one micron, at least two of the widths being different; and

forming a conductive line over respective active areas to provide individual transistor gates, [the] wherein transistors corresponding to the active areas having the different widths [having] have different threshold voltages.

37. (Amended) The transistor assembly of claim 34, wherein one of the individual transistors comprises a portion of precharge circuitry for dynamic random access memory circuitry.

38. (Amended) The transistor assembly of claim 34, wherein one of the individual transistors comprises a pass transistor.

39. (Amended) The transistor assembly of claim 34, wherein one of the individual transistors comprises a portion of sense amplifier circuitry for dynamic random access memory circuitry and has a lower threshold voltage V_{tl}.

40. (Amended) The transistor assembly of claim 34, wherein some of the individual transistors are joined together in a parallel configuration.

41. (Amended) Dynamic random access memory circuitry comprising:

a substrate having a memory array area for supporting memory circuitry and a peripheral area for supporting peripheral circuitry;

a plurality of active areas within the peripheral area having widths [defined by shallow trench isolation regions] of no greater than about one micron, the widths being defined by shallow trench isolation regions, at least some of the widths being different; and

conductive lines disposed over the plurality of active areas to provide individual transistors, those transistors whose widths are different having different threshold voltages from one another.

44. (Amended) A transistor assembly comprising:

an active area;

a plurality of spaced-apart shallow trench isolation regions received by the active area and defining active sub-areas therebetween, individual active sub-areas having respective widths, at least one of the widths being no greater than about one micron and at least one other sub-area having a width which is different from the one width; and

a gate line extending over the one and the other sub-area and defining, in part, separate transistors, wherein each of the separate transistors [have] has a different threshold voltage [voltages].

45. (Amended) The transistor assembly of claim 44, [further comprising a gate line extending over a plurality of the active sub-areas defining a plurality of transistors,] <u>wherein</u> each active sub-area width of an associated transistor [being] <u>is</u> no greater than about one micron.

46. (Amended) The transistor assembly of claim 44, [further comprising a gate line extending over a plurality of the active sub-areas defining a plurality of transistors,] <u>wherein</u> each active sub-area width of an associated transistor [being] <u>is</u> no greater than about one micron, wherein more than two [of the plurality of] <u>separate</u> transistors have different threshold voltages.

50. (Amended) The transistor assembly of claim 49, further comprising a sense amplifier formed from <u>a</u> pair of transistors, each of the pair having a gate that is cross-coupled to a drain of another of the pair, sources of the pair being coupled to the common node.

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